Abstract

The present invention stacks chip scale-packaged integrated circuits (CSPs) into low profile modules that conserve PWB or other board surface area. Low profile structures provide connection between CSPs of the stacked module and between and to the flex circuitry. Low profile contacts are created by any of a variety of methods and materials including, for example, screen paste techniques and use of high temperature solders, although other application techniques and traditional solders may be employed for creating low profile contacts in the present invention. A consolidated low profile contact structure and technique is provided for use in alternative embodiments of the present invention. Multiple numbers of CSPs may be stacked in accordance with the present invention. The CSPs employed in stacked modules devised in accordance with the present invention are connected with flex circuitry. That flex circuitry may exhibit one or two or more conductive layers. In some preferred embodiments, a form standard provides a physical form that allows many of the varying package sizes found in the broad family of CSP packages to be used to advantage while employing a standard connective flex circuitry design. In other embodiments, a heat spreader is disposed between the CSP and the flex circuitry thus providing an improved heat transference function without the standardization of the form standard, while still other embodiments lack either a form standard or a heat spreader and may employ, for example, the flex circuitry as a heat transference material.